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| 10/720,565 | 11/24/2003 | John G. McBride | 200310795-1 | 5728 |

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| EXAMINER | |
|---|---|
| THORNEWELL, KIMBERLY A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2128 | |

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/720,565 | MCBRIDE, JOHN G. | |
| | Examiner | Art Unit | |
| | Kimberly Thornewell | 2128 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-12 are pending in the present application.

### *Claim Interpretation*

2. The claimed "hypermatrix" has not been defined in claims or in the specification. Therefore a hypermatrix is interpreted to be a lookup table that stores simulated performance results (based on specification paragraph 12 lines 5-6).

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first two paragraphs of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 9-12 are directed to a system; however, there is no support in the specification for a system implementation of the invention.

5. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 3, 4, 9 and 10 claim the term "hypermatrix," which has not been expressly defined in the specification. Claims 2, and 5-7 are rejected because they are dependent on claim 1. Claims 11 and 12 are rejected because they are dependent on claim 9.
6. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the specification, the Applicant's preferred embodiment covers the use of FET gate widths, FET gate lengths, capacitance, resistance, and inductance as parameters. The Applicant only mentions the use of structural beam widths, lengths, heights, structural types, and materials as another embodiment. Furthermore, in the claim the Applicant implies that all parameters must be present in order to be selected. However, this is not covered by the specification because in the specification the Applicant implies that the parameters are present in the alternative (see paragraph 18, lines 2-5, emphasis on "and/or" on line 3). It is unclear whether all parameters must be present for selection, or if any combination of the parameters may be present.
7. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention. The preferred embodiment of the specification covers VLSI design and electronic circuit design, while civil engineering and mechanical engineering design are mentioned as other embodiments. Similar to claim 2 above, the claim implies that all fields of design must be present for selection. However, this is not covered by the specification because the specification only covers the fields of design in the alternative (see paragraph 18 lines 1-2). It is unclear whether all fields of design must be present for selection, or if any combination of the fields of design may be present.

8. Claims 9-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 9-12 are directed to a system for accurate design rule checking, comprising means for performing steps of a method. It is unclear what is meant by the means for each function, as they are not covered in the specification.

### *Claim Rejections - 35 USC § 101*

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 1-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The ideas claimed are abstract in nature and the Applicant has not set forth a tangible

invention. Claims 1-8 are directed to a method for accurate design rule evaluation. Even though the hypermatrix in claim 1 is stored in memory, the specification does not cover the fact that the memory is concrete, and could be a virtual memory. Claim 8 is directed to performing the method using computer executable software code, and it would be impossible to realize a concrete memory in computer executable software code. Claims 9-12 are directed to a system that performs an abstract method. There is no tangible result obtained by using the system to perform the method.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1, 3-5, and 7-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsukuda, US PreGrant Publication US 2003/0037308 A1.

As per claim 1, Tsukuda discloses a method for accurate design rule evaluation, said method comprising:

**constructing sample design portions in a simulator** (paragraph 16 lines 5-7, portions taught as each individual layout pattern);

**sweeping simulated design parameters independently** (figure 18, paragraph 22);

**generating a hypermatrix of results of said sweeping** (taught as the L/S matrix, figure 18, paragraph 21); and

**storing said hypermatrix in memory** (figure 15, reference 203).

As per claim 3, Tsukuda further discloses the method of claim 1 further comprising:

**extracting said swept parameters as indices** (paragraph 111); and

**retrieving said results from said pregenerated hypermatrix** (paragraph 97 lines 5-10, paragraph 98 lines 1-4).

As per claim 4, Tsukuda further discloses the method of claim 3 wherein said retrieving comprises **looking up said results in said hypermatrix using said indices** (paragraph 114).

As per claim 5, Tsukuda further discloses the method of claim 3 further comprising **using said results to evaluate an individual design** (paragraph 115, emphasis on lines 8-10 for evaluation).

As per claim 7, Tsukuda further discloses the method of claim 1 wherein **said hypermatrix of results is a mathematical representation**

**relating an array of mathematical functions of multiple independent variables** (paragraph 23, functions taught as difference between original and finished dimensions, defocus margin, and exposure margin) **to arrays of said multiple independent variables** (paragraph 22, variables taught as line widths).

As per claim 8, Tsukuda further discloses the method of claim 1 wherein **said method is performed using computer executable software code** (paragaraph 122, computer executable code taught as the layout verification program).

As per claim 9, Tsukuda discloses a system for accurate design rule checking, said system comprising:

**means for constructing sample design portions in a simulator** (paragraph 16 lines 5-7, portions taught as each layout pattern);

**means for sweeping simulated design parameters independently** (figure 18, paragraph 22); and

**means for generating a hypermatrix of results of said sweeping** (taught as the L/S matrix, figure 18, paragraph 21).

As per claim 10, Tsukuda further discloses the system of claim 9 further comprising: **means for retrieving said results from said**

**generated hypermatrix** (paragraph 97 lines 5-10, paragraph 98 lines 1-4).

As per claim 11, Tsukuda discloses the system of claim 10 further comprising:

**means for using said results to evaluate an individual design** (paragraph 115, emphasis on lines 8-10 for evaluation).

As per claim 12, Tsukuda discloses the system of claim 10 further comprising: **means for extracting said swept parameters as indices** (paragraph 111).

***Claim Rejections - 35 USC § 103***

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukuda in view of Sebastian et al., US Patent no. 5,822,206, and further in view of Regan, US Patent no. 6,756,242.

As per claim 2, Tsukuda does not disclose expressly the design parameters being selected from structural beam widths, beam lengths,

beam heights, structural types, materials, FET gate widths, FET gate lengths, capacitance, resistance, and inductance.

Sebastian discloses a design rule checking method (column 7 lines 50-55) for part design, comprising selecting parameters such as **beam widths, beam lengths, beam heights** (column 12 lines 66-67, column 13 lines 1-3, beam design taught in column 20 lines 25-31), **structural types** (figure 7 reference 102), **materials** (column 24 lines 15 and 22).

Regan discloses a design method for modifying a **FET gate widths, FET gate lengths** (column 5 line 46), **capacitance, resistance and inductance** (column 4 lines 33-38).

It would have been obvious to one of ordinary skill in the art of design rule checking, at the time of the present invention, to modify the teachings of Tsukuda relating to design rule checking using a hypermatrix, with the teachings of Sebastian relating to design parameters dealing with civil and mechanical engineering, and further modify the teachings of Tsukuda with the teachings of Regan releting to FET circuit design in order to achieve the claimed invention. The motivation for doing so would have been allow more flexibility in component design by making the method accommodate for different engineering fields (Sebastian column 5 lines 11-21, allowing for both civil and mechanical engineering).

15. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukuda in view of Sebastian et al., US Patent no. 5,822,206, and further in view of Wood, US Patent Application 2005/0010883.

As per claim 6, Tsukuda discloses the individual design being an **electronic circuit design** (paragraph 28). Tsukuda does not disclose expressly the individual design being selected from VLSI design, civil engineering design, and mechanical engineering design.

Sebastian discloses his design rule checking method being applied to **civil engineering design** (column 26 lines 2-5) and **mechanical engineering design** (column 5 lines 14-21).

Wood discloses his design rule checking method being applied to **VLSI design** (paragraph 1).

It would have been obvious to one of ordinary skill in the art of design rule checking, at the time of the present invention, to modify the teachings of Tsukuda relating to design rule checking using a hypermatrix, with the teachings of Sebastian relating to design parameters dealing with civil and mechanical engineering, and further modify the teachings of Tsukuda with the teachings of Wood relating to VLSI circuit design in order to achieve the claimed invention. The motivation for doing so would have been allow more flexibility in component design by making the method accommodate for different engineering fields (Sebastian column 5 lines 11-21, allowing for both civil and mechanical engineering).

***Conclusion***

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

    i. US Patent no. 5,208,765, issued to Turnbull on 5/4/93, discloses a method for design rule checking using a control matrix.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly Thornewell whose telephone number is (571)272-6543. The examiner can normally be reached on 8am-4:30pm M-F.

    If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

    Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly A. Thornewell
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Art Unit 2128